Patent Claims

1. An integrated circuit arrangement (120), having an electrically insulating insulating region, and having at least one sequence of regions which forms a capacitor (124) and which contains, in the order specified:
an electrode region (34) near the insulating region,
a dielectric region (46), and
an electrode region (56) remote from the insulating region,
the insulating region being part of an insulating layer (14) arranged in a plane,
the capacitor (124) and at least one active component (122) of the integrated circuit arrangement (120) being arranged on the same side of the insulating layer (14), and the electrode region (34) near the insulating region and the active region (82) of the component (122) being arranged in a plane which lies parallel to the plane in which the insulating layer (14) is arranged.

2. The circuit arrangement (120) as claimed in claim 1, wherein the electrode region (34) near the insulating region is a monocrystalline region, preferably a doped semiconductor region,
and/or wherein the electrode region (34) near the insulating region and/or the active region (82) has a thickness of less than one hundred nanometers or less than fifty nanometers,
and/or wherein the active region (82) is a monocrystalline region, preferably a semiconductor region which is doped or undoped,
and/or wherein the insulating layer (14) adjoins, at one side, a carrier substrate (12), preferably a carrier substrate which contains a semiconductor

material or comprises a semiconductor material, in particular silicon or monocrystalline silicon,
and/or wherein the insulating layer (14) adjoins the electrode region (34) near the insulating region at the other side,
and/or wherein the boundary areas preferably lie completely in two mutually parallel planes,
and/or wherein the insulating layer (14) contains an electrically insulating material, or comprises an electrically insulating material, preferably an oxide, in particular silicon dioxide,
and/or wherein the active component (122) is a transistor, preferably a field-effect transistor, in particular a FinFET.

3. The circuit arrangement (120) as claimed in claim 1 or 2, wherein the dielectric region (46) contains silicon dioxide or comprises silicon dioxide,
and/or wherein the dielectric region (46) comprises a material having a dielectric constant of greater than four or greater than ten or greater than fifty,
and/or wherein the electrode region (56) remote from the insulating region contains silicon, preferably polycrystalline silicon, or comprises silicon, preferably polycrystalline silicon,
and/or wherein the electrode region (56) remote from the insulating region contains a metal or comprises a metal,
and/or wherein the electrode region (56) remote from the insulating region contains a low-impedance material, preferably titanium nitride, tantalum nitride, rubidium or highly doped silicon-germanium,
and/or wherein the electrode region (56) remote from the insulating region adjoins a region containing metal-semiconductor compounds, in particular a silicide region (96).

4. The circuit arrangement (120) as claimed in one of the preceding claims, wherein the dielectric region (46) and the electrode region (56) remote from the insulating region are arranged at two, at three, at four or at five side areas or at more than five side areas of the electrode region (34) near the insulating region,
and/or wherein the electrode region (34) near the insulating region contains a multiplicity of webs whose web height is preferably larger than the web width, preferably at least twice as large.

5. The circuit arrangement (120) as claimed in one of the preceding claims, characterized by at least one field-effect transistor (122), whose channel region (82) is the active region, the channel region (82) preferably being undoped,
and/or whose control electrode (54) contains the same material and/or material of the same dopant concentration as the electrode region (56) remote from the insulating region,
and/or whose control electrode insulation region (42, 44) contains the same material and/or a material having the same thickness as that of the dielectric region (46),
and/or whose control electrode insulation region (42, 44) contains a different material and/or a material having a different thickness than the dielectric region (46).

6. The circuit arrangement (120) as claimed in claim 5, wherein the field-effect transistor (122) contains at least one web,
and/or wherein a plurality of control electrodes (54) are arranged at mutually opposite sides of the web (30a), preferably two or three control electrodes,

and/or wherein at least one control electrode (54) adjoins a region containing metal-semiconductor compounds, in particular a silicide region (92),
and/or wherein a connecting region electrically connects the control electrodes (54), the connecting region being isolated from the channel region preferably by a thick insulating region (18, 20), which preferably has an insulating thickness which is greater than the thickness of control electrode insulation regions (42, 44),
and/or the connecting region comprising the same material and/or having the same doping level as the electrode region (56) remote from the insulating region.

7. The circuit arrangement (120) as claimed in claim 5 or 6, wherein one terminal region or both terminal regions (70, 22) of the field-effect transistor (122) adjoin the insulating layer (14),
and/or wherein at least one terminal region (70, 72) adjoins a region containing a metal-semiconductor compound, preferably a silicide region (90, 94),
and/or wherein the terminal regions (70, 72) have a larger thickness than the active region (72).

8. The circuit arrangement (120) as claimed in one of claims 5 to 7, wherein spacers (60b, 60c) are arranged on both sides of the control electrodes (54), which spacers preferably contain a different material than the electrode layer, preferably silicon nitride, or which spacers comprise a different material than the electrode layer, preferably silicon nitride,
and/or wherein a spacer (60d) is arranged at at least one side of the electrode region (56) remote from the insulating region, which spacer contains a different material, preferably silicon nitride, or comprises a

different material than the electrode layer (50), preferably silicon nitride,
and/or wherein a spacer (60c) arranged at a control electrode (54) and a spacer (60d) arranged at the electrode region (56) remote from the insulating region touch one another.

9. The circuit arrangement (120) as claimed in one of claims 5 to 8, wherein a terminal region (72) of the field-effect transistor (122) and the electrode region (34) of the capacitor (124) which is near the insulating region adjoin one another and have an electrically conductive connection at the boundary,
and/or wherein the terminal region (72) which adjoins the electrode region (34) does not adjoin a region containing a metal-semiconductor compound,
and/or wherein the other terminal region (70) adjoins a region containing a metal-semiconductor compound.

10. The circuit arrangement (120) as claimed in claim 9, wherein that side of the electrode region (34) near the insulating region which adjoins the terminal region (72) is longer than a side of the electrode region (34) near the insulating region which lies transversely with respect to said side, preferably being at least twice as long or at least five times as long,
the transistor (122) preferably having a transistor width which is a multiple of the minimum feature size (F), preferably more than three-fold or more than five-fold,
or wherein a side of the electrode region (34) near the insulating region which lies transversely with respect to that side of the electrode region (34) near the insulating region which adjoins the terminal region (72) is longer than the side adjoining the terminal

region (72), preferably at least twice as long or at least five times as long,
the transistor (122) preferably having a transistor width which is less than three times the minimum feature size (F), preferably less than twice the minimum feature size (F).

11. The circuit arrangement (120) as claimed in one of the preceding claims, wherein the circuit arrangement contains at least one processor, preferably a microprocessor,
and/or wherein the capacitor (124) and the active component (122) form a memory cell (120), in particular in a dynamic RAM memory unit,
and/or wherein a memory cell contains either a capacitor (122) and only one transistor (122) or a capacitor (Cs) and more than one transistor (M1 to M3), preferably three transistors (M1 to M3).

12. A method for fabricating an integrated circuit arrangement (120) with a capacitor (124), in particular a circuit arrangement (120) as claimed in one of the preceding claims,
in which the following method steps are performed without any restriction by the order specified:
provision of a substrate (10) containing an insulating layer (14) made of electrically insulating material and a semiconductor layer (16),
patterning of the semiconductor layer (16) in order to form at least one electrode region (34) for a capacitor and in order to form at least one active region (82) for a transistor (122),
after the patterning of the semiconductor layer (16) production of at least one dielectric layer (42, 44, 46), after the production of the dielectric layer (42, 44, 46) production of an electrode layer (50),

formation of an electrode (56) of the capacitor (124) which is remote from the insulating region in the electrode layer (50).

13. The method as claimed in claim 12, characterized by the following steps:
application of at least one insulating layer (18, 20) to the semiconductor layer (16) prior to patterning, preferably a silicon nitride layer (18) and/or an oxide layer (20) having a first thickness,
and/or doping of the electrode (34) near the insulating region, preferably before the production of the dielectric layer (42, 44, 46),
and/or production of the dielectric layer (42, 44, 46) at the same time as a dielectric layer at the active region (82) of the transistor (122),
and/or formation of a control electrode (54) of the transistor (122) at the same time as the formation of the electrode region (56) remote from the insulating region.

14. The method as claimed in claim 12 or 13, characterized by the following steps:
production of an auxiliary layer (52) after the production of the electrode layer (50), preferably an auxiliary layer having a larger thickness than the oxide layer (18, 20),
and/or patterning of the electrode region (56) remote from the insulating region and/or of a control electrode (54) of the transistor using the auxiliary layer (52) as a hard mask.

15. The method as claimed in one of claims 12 to 14, characterized by the following steps:
application of a further auxiliary layer (60) after the patterning of a control electrode (54) of the transistor (142), preferably a silicon nitride layer,

and/or anisotropic etching of the further auxiliary layer (60).

16. The method as claimed in one of claims 12 to 15, characterized by the following steps:
repeated patterning of the insulating layer (18, 20), preferably the thickness of the auxiliary layer (52) being reduced and/or the auxiliary layer (52) not being completely removed, however,
and/or anisotropic etching of the further auxiliary layer (60) after the patterning of the insulating layer (20).

17. The method as claimed in one of claims 12 to 16, characterized by the following steps:
carrying out of a selective epitaxy on uncovered regions made of semiconductor material (16) after the formation of the electrode region (56) remote from the insulating region and/or after the patterning of a control electrode (54) of the transistor (122),
and/or doping of terminal regions (70, 72) of the transistor (122) after the formation of the electrode region (56) remote from the insulating region and/or after the patterning of the control electrode (54) and preferably after the epitaxy.

18. The method as claimed in one of claims 12 to 17, characterized by the following steps:
removal of the auxiliary layer (52), preferably after the patterning of the insulating layer (18, 20) and/or after the carrying out of the selective epitaxy,
and/or selective formation of a metal-semiconductor compound, in particular selective silicide formation, on the electrode layer (54) and/or on uncovered semiconductor regions (16).